This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Original): A data array system for providing a host computer device having a host bus redundant access to a data storage device, comprising:

an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and

a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link.

Claim 2 (Original): The system of Claim 1, wherein the host bus is a peripheral component interconnect (PCI) bus.

Claim 3 (Original): The system of Claim 2, wherein the active and the standby controllers are PCI-compliant devices.

Claim 4 (Original): The system of Claim 1, wherein the standby controller includes a queue for storing a signal identifier and wherein the messaging mechanism of the active controller writes the signal identifier over the host bus to the standby queue to provide processing information for the transmitted messages and data.

Claim 5 (Original): The system of Claim 4, wherein standby controller includes a messaging mechanism configured to process the signal identifier in response to an interrupt from the active controller and to process the stored messages and data based on the signal identifier.

Claim 6 (Original): The system of Claim 5, wherein the signal identifier indicates the stored messages and data as a message-only transfer, a message-with-data transfer, or a message-with-partial data transfer.

Claim 7 (Original): The system of Claim 6, wherein the standby messaging mechanism moves data in the data buffer to memory as part of the processing of the stored messages and data.

Claim 8 (Original): The system of Claim 7, wherein the active controller includes a reply queue and the standby messaging mechanism replies to the transmitted messages and data by writing a reply message to the reply queue indicating messaging can be transmitted by the active controller.

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Claim 9 (Currently amended): A method for providing inter-controller communications between an active controller and a standby controller configured for redundant communications between a host and a storage device and linked to a host bus,

comprising:

at the active controller, building a message;

with the active controller, transferring the message to the standby controller via the host bus;

with the active controller, writing to a command/reply queue at the standby controller;

with the standby controller, checking the command/reply queue for a next message; and

upon detecting the next message, processing with the standby controller the transferred message.

Claim 10 (Original): The method of Claim 9, further including driving an interrupt with the active controller to standby controller and wherein the checking is performed in response to the standby controller sampling the interrupt.

Claim 11 (Original): The method of Claim 10, further including with the active controller transferring data with the message, and wherein the transferred message indicates a presence or absence of the data.

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Claim 12 (Original): The method of Claim 11, wherein the message defines the data as all or partial and wherein the standby controller stores the data based on the all or partial data definition.

Claim 13 (Original): The method of Claim 9, further including after the processing, with the standby controller writing to a reply queue at the active controller to indicate the processing is complete.

Claim 14 (Previously presented): A data storage system with redundant data storage, comprising:

a host processor;

an active controller controlling access by the host processor to data storage devices;

a standby controller controlling access by the host processor to the data storage devices; and

a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus.

Claim 15 (Original): The system of Claim 14, wherein the standby controller includes a command/reply queue for registering receipt of new messages and a message buffer for storing messages, and wherein the active redundancy mechanism transfers messages to the message buffer of the standby controller and writes to the command/reply queue to indicate the transmittal of the messages.

Claim 16 (Original): The system of Claim 15, wherein the active redundancy mechanism asserts an interrupt to the standby controller over the host bus and the standby redundancy mechanism responds to the interrupt by checking the command/reply queue.

Claim 17 (Original): The system of Claim 14, wherein the standby controller includes a data buffer and wherein the active redundancy messaging mechanism transfers data corresponding to the message over the host bus to the data buffer.

Claim 18 (Original): The system of Claim 17, wherein the standby redundancy messaging mechanism transfers the data from the data buffer to another memory device to enable receipt of additional data and transmits a signal to the active controller upon completion of the transfer of the data out of the data buffer.

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Claim 19 (Original): The system of Claim 18, wherein the signal includes writing to a reply queue at the active controller and transmitting an interrupt to the active controller.

Claim 20 (Original): The system of Claim 14, wherein the host bus is a peripheral component interconnect (PCI) bus and the active and standby controllers are PCI-compliant devices.

Claim 21 (Currently amended): A method for providing inter-controller communications between an active controller and a standby controller configured for redundant communications between a host and a storage device and linked to a host bus, comprising:

at the standby controller, specifying a range of memory in the standby controller as an interrupt range;

with the active controller, writing data via the host bus to the interrupt range of the standby controller; and

at the standby controller, driving a local interrupt.

Claim 22 (Original): The method of Claim 21, wherein the interrupt driving is performed with a memory controller in the standby controller.

Claim 23 (Original): The method of Claim 21, further including after the interrupt driving, with the standby controller writing to a reply queue at the active controller.

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Claim 24 (Previously presented): A computing device comprising:

a host central processing unit (CPU);

a host bus communicatively coupled to the host CPU;

at least one data storage device;

an active controller linked to the host bus and the at least one data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and,

a standby controller linked to the host bus and the at least one data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link configured to transfer data and message information between the active and standby controllers and wherein upon a failure of the active controller the inter-controller-link provides both data and message transfer within the computing device such that the host CPU can cause the standby controller to access data from the at least one data storage device.

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Claim 25 (Previously presented): A data array system for providing a host computer device having a host bus redundant access to a data storage device, comprising:

an active controller sub-system linked directly to the host bus and the data storage device, the active controller sub-system including a messaging mechanism for transmitting messages and data over the host bus; and,

a standby controller sub-system linked directly to the host bus and the data storage device, the standby controller sub-system including message and data buffers for storing the messages and data, whereby the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the host computing device maintains access to the data storage device.

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